USER GUIDE

SMARC-sXAS

User Guide Rev. 1.0

JUMPtec

Table of Contents

1. General Information 3
1.1 Disclaimer 3
1.2 Intended Use 4
1.3 Terms and Conditions 5
1.4 Customer Support 5
1.5 Customer Service 5
1.6 Customer Comments 5
1.7 Symbols 6
1.8 For Your Safety 7
1.9 High Voltage Safety Instructions 7
1.10 Special Handling and Unpacking Instruction 7
1.11 Lithium Battery Precautions 8
1.12 General Instructions on Usage 8
1.13 Quality and Environmental Management 9
1.13.1 Disposal and Recycling 9
1.13.2 WEEE Compliance 9
2. Introduction 10
2.1 Product Naming Clarification 10
2.2 Description 10
2.3 SMARC-sXAS Module 11
3. Product specification 12
3.1 Module Variants 12
3.1.1 Commercial Temperature Grade Modules (0°C to +60°C) 12
3.1.2 Industrial Temperature Grade Modules (E2, -40°C to +85°C) 12
3.2 Accessories 12
3.2.1 Cooling 12
3.2.2 Evaluation Carrier 12
3.2.3 Mounting 13
3.3 Functional Specification 13
3.3.1 Technical Data 13
3.3.2 Block Diagram 14
3.3.3 Top Side 15
3.3.4 Bottom Side 16
3.3.5 Processor (CPU) 16
3.3.6 Plattform Controller Hub (PCH) 18
3.3.7 System Memory 18
3.3.8 HSIO Mapping 18
3.4 Interfaces 18
3.4.1 PCIe 18
3.4.2 USB 18
3.4.3 SATA 3.0 19
3.4.4 Graphics Interfaces 20
3.4.5 Audio Interface 20
3.4.6 UART Interfaces 20
3.4.7 Boot SPI Interface 21
3.4.8 General Purpose SPI (GSPI) / eSPI 21
3.4.10 I2C 22
3.4.11 GPIO 22

3.4.12 SMB 23
3.3.13 CAN Bus 23
3.4.14 Ethernet 23
3.4.15 MIPI CSI 23
3.5 Features 24
3.5.1 ACPI Power States 24
3.5.2 Embedded Controller 25
3.5.3 Trusted Platform Module 25
3.5.4 Watchdog 25
3.5.5 RTC 26
3.5.6 eMMC Flash Memory 26
3.5.7 EEPROM 26
3.5.8 Features on Request 27
3.6 Electrical Specification 27
3.7 Thermal Management 28
3.7.1 Heatspreader 28
3.7.2 Thermal Sensors 29
3.7.3 Fan Connector 29
3.8 Mechanical Specification 29
3.8.1 Mechanical Drawings 29
3.9 Environmental Specification 30
3.10 Compliance 30
3.11 MTBF 32
4. Pin Definitions 33
4.1.1 Pinout of SMARC Connector (Top Side) 33
4.1.2 Pinout of SMARC Connector (Bottom Side) 46
5. UEFI BIOS 62
5.1 Starting the UEFI BIOS 62
5.2 Navigating the UEFI BIOS 63
5.3 Setup Menus 63
5.4 Getting Help 64
5.5 UEFI Shell 65
5.5.1 Entering the UEFI Shell 65
5.5.2 Exiting the UEFI Shell 65
5.6 UEFI Shell Scripting 66
5.6.1 Startup Scripting 66
5.6.2 Create a Startup Script 66
5.6.3 Example of Startup Scripts 66
5.7 Firmware Update 66
6. Technical Support 67
6.1 Warranty 67
6.2 Returning Defective Material 67
7. Document Revision 69
List of Acronyms 70

1. General Information

1.1 Disclaimer

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1.2 Intended Use

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, “HIGH RISK APPLICATIONS”).

You understand and agree that your use of JUMPtec devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any JUMPtec hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the JUMPtec device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested JUMPtec products, and other materials) is provided for reference only.

Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Follow the “General Safety Instructions” supplied with the product.

You find the most recent version of the “General Safety Instructions“ online in the download area of this product on our JUMPtec website.

This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact JUMPtec Support.

1.3 Terms and Conditions

JUMPtec warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.jumptec.com/en/terms-and-conditions.

JUMPtec sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.jumptec.com/en/terms-and-conditions.

For contact information, please visit our website CONTACT US.

1.4 Customer Support

Find JUMPtec contacts by visiting: https://www.jumptec.com/en/service-support.

1.5 Customer Service

As a trusted technology innovator and global solutions provider, JUMPtec extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables JUMPtec to provide exceptional peace of mind to build and maintain successful products. For more details on JUMPtec's service offerings such as: enhanced repair services, extended warranty, training academy, and more visit https://www.jumptec.com/en/service-support.

1.6 Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact JUMPtec Support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

1.7 Symbols

The following symbols may be used in this user guide of SMARC-sXAS

Simple Box

Info-Box

Important-Box

Alert-Box

Tip-Box

Help-Box

Todo-Box

Download-Box

1.8 For Your Safety

Your new JUMPtec product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new JUMPtec product, you are requested to conform with the following guidelines.

1.9 High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

Electric Shock!

Before installing a non hot-swappable JUMPtec product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product. Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

1.10 Special Handling and Unpacking Instruction

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes

unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

1.11 Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer’s instructions.

1.12 General Instructions on Usage

In order to maintain JUMPtec’s product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by JUMPtec and described in this user guide or received from JUMPtec Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account. In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product, then re-pack it in the same manner as it was delivered. Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

1.13 Quality and Environmental Management

JUMPtec aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding JUMPtec's quality and environmental responsibilities, visit https://www.jumptec.com/en/about-jumptec/quality.

1.13.1 Disposal and Recycling

JUMPtec's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.13.2 WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with JUMPtec.

JUMPtec follows the WEEE directive.

You are encouraged to return our products for proper disposal.

2. Introduction

This user guide describes the Smart Mobility Architecture (SMARC) Computer-On-Module SMARC-sXAS made by JUMPtec and focuses on describing the module's special features. JUMPtec recommends users to study this user guide before powering on the module.

2.1 Product Naming Clarification

SMARC® defines a Computer-On-Module (COM), with all the components necessary for a bootable host computer, packaged as a super component. The product name for JUMPtec SMARC® Computer-On-Modules consists of:

Standard short form	Module size	Architecture	Processor family identifier	Available temperature variants
SMARC-	s=small l=large	X = x86 A = ARM	AS = Amston Lake AL = Apollo Lake etc.	(none=) Commercial Extended (E1) Industrial (E2)

Table 1: SMARC® Product Naming Clarification

2.2 Description

The SMARC™ standard was developed especially for new modules with SOC processors. Modules with this interfaces are characterized by the extremely flat form factor. The SMARC or MXM 3.0 connector comes with 314 pins and a construction height of just 4.3 millimeters. The connector is also available in a shock- and vibration resistant version for rough environmental conditions. Furthermore, the standard integrates dedicated interfaces for the latest processors. OEMs profit from minimized design effort and low Bill of Material (BoM) costs. SMARC™ defines two different module sizes in order to offer a high level of flexibility regarding different mechanical requirements.

2.3 SMARC-sXAS Module

The SMARC-sXAS is a SMARC half-size module using the Intel® Atom®/Pentium®/Celeron® 7xxx processor family and based on the latest SMARC 2.2 specification.

Figure 1: SMARC-sXAS

General features are:

- Up to 16 GByte LPDDRx memory down with in-band ECC support
- Dual LVDS, HDMI, DP++
- 1x USB 3.2
- 6x USB 2.0
- PCIe Gen. 3
- eMMC onboard
- Industrial grade temperature

3. Product specification

3.1 Module Variants

3.1.1 Commercial Temperature Grade Modules (0°C to +60°C)

Different versions containing commercial SKUs can be realized on project base. Please get in contact with GSS for further details.

3.1.2 Industrial Temperature Grade Modules (E2, -40°C to +85°C)

Part No.	SoC	Cores	Frequ.	Memory	Flash	Op. Temp.
51018-0432-R1-2	x7211RE	2 core	1.0GHz	4GB LPDDR5 memory down	32GB eMMC TLC	industrial temperature
51018-0432-R2-2	x7213RE	2 core	2.0GHz	4GB LPDDR5 memory down	32GB eMMC TLC	industrial temperature
51018-0432-R2-4	x7433RE	4 core	1.5GHz	4GB LPDDR5 memory down	32GB eMMC TLC	industrial temperature
51018-0832-R2-8	x7835RE	8 core	1.3GHz	8GB LPDDR5 memory down	32GB eMMC TLC	industrial temperature

Table 2: Product Number for Industrial Grade Modules (-40°C to +85°C)

3.2 Accessories

Accessories are product specific or SMARC® specific accessories. For more information, contact your local JUMPtec Sales Representative or JUMPtec Inside Sales.

3.2.1 Cooling

A standard heat spreader solution can be used, which are available in a non-threaded (through hole) version.

JUMPtec PN	Product Name	Description
51018-0000-99-1	HSP SMARC-sXAS	Heatspreader for SMARC-sXAS
51099-0000-99-1	SMARC PASSIVE UNI COOLER (W/O HSP)	SMARC Passive Uni Cooler

Table 3: Cooling Equipment SMARC-sXAS available from JUMPtec

3.2.2 Evaluation Carrier

JUMPtec PN	Product Name	Description
51301-0000-00-0	SMARC Evaluation Carrier 2.1	SMARC Evaluation Carrier for SMARC modules according to the SMARC 2.1 standard (without SMARC module)

Table 4: Evaluation Carrier from JUMPtec

3.2.3 Mounting

JUMPtec PN	Product Name	Description
51117-0000-00-0	SMARC MOUNTING KIT	Mounting Kit for SMARC modules

Table 5: Mounting Kit from JUMPtec

3.3 Functional Specification

3.3.1 Technical Data

COMPLIANCE	SMARC module 2.2
DIMENSIONS (H X W X D)	82 x 50 mm
CPU	Intel Amston Lake SKUs – Industrial RE-Series
CHIPSET	-
MAIN MEMORY	Up to 16 GByte LPDDR5 memory down with inband ECC support
GRAPHICS CONTROLLER	Gen 12 IGFX
ETHERNET	Up to 2.5GbE
STORAGE	1x SATA 6Gb/s
FLASH ONBOARD	up to 256 GByte eMMC (TLC, pSLC optional)
PCI EXPRESS®	up to 4x PCIe x1
PANEL SIGNAL	1x HDMI (on request DP++), 1x DP++, 1x Dual LVDS (on request eDP)
USB	1x USB 3.2, 6x USB 2.0
SERIAL	4x UART (2x RX/TX only)
OTHERS FEATURES	HD Audio, I²C, 2x SPI, 14x GPIOs
SPECIAL FEATURES	Trusted Platform Module TPM 2.0 Industrial Temperature Grade versions
FEATURES ON REQUEST	eMMC: up to 85 GByte pSLC RAM: from 2 GByte to 16 GByte LPDDR4
BIOS	AMI UEFI
OPERATING SYSTEM	Windows® 10 (IOT) Enterprise x64, Windows® 11, Linux
POWER SUPPLY	5V only! No Widerange
TEMPERATURE	Industrial grade: -40°C to +85°C operating, -40 °C to +85 °C non-operating
HUMIDITY	93 % relative Humidity at 40 °C, non-condensing (according to IEC 60068-2-78)

Table 6: Technical Data

3.3.2 Block Diagram

The block diagram shows all availabale SMARC-sXAS interfaces.

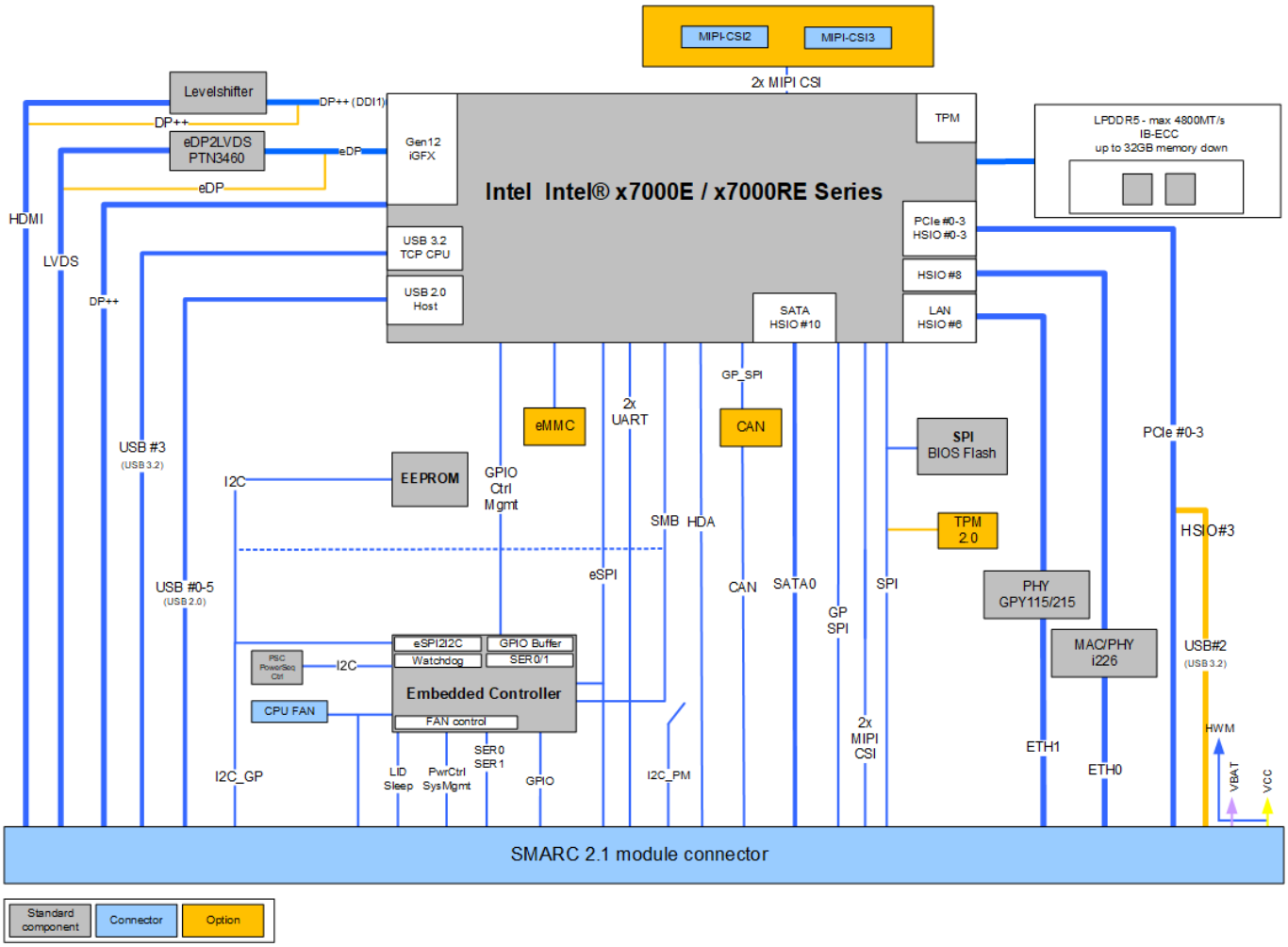


Figure 2: SMARC-sXAS Blockdiagram

3.3.3 Top Side

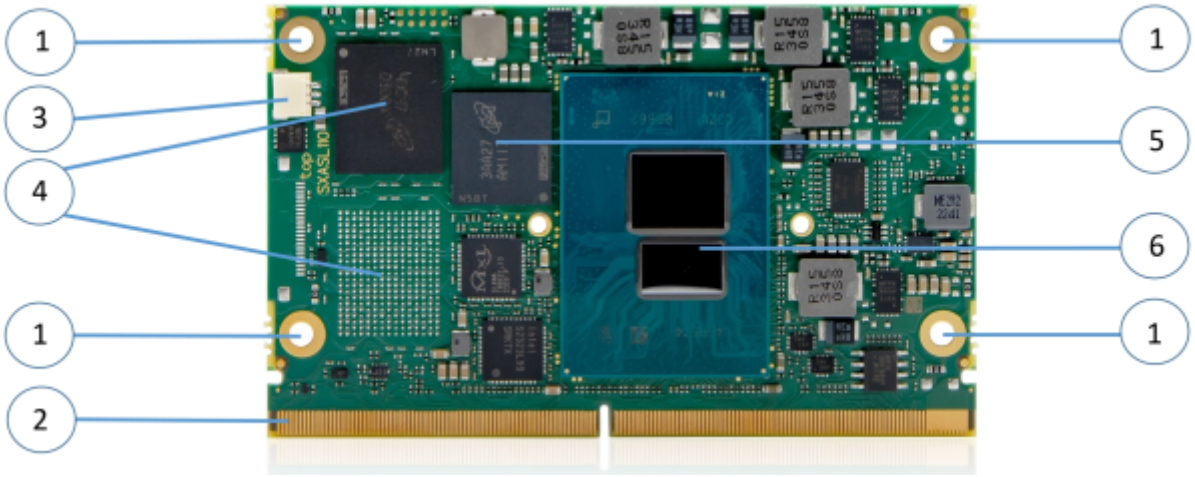


Figure 3: SMARC-sXAS Front Side

1. Mounting Holes
2. SMARC Connector
3. Fan Connector
4. Optional eMMC
5. LPDDR5
6. SoC

3.3.4 Bottom Side

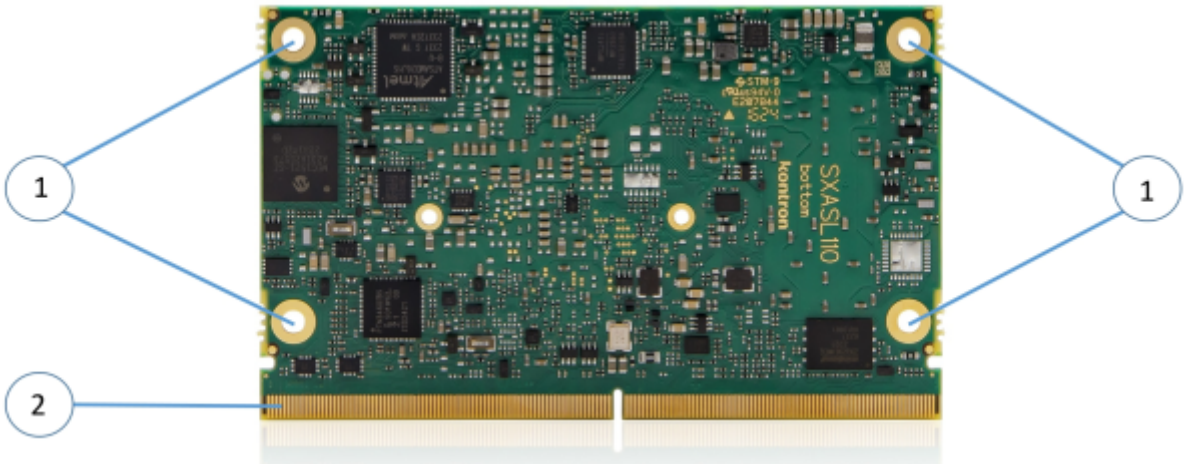


Figure 4: SMARC-sXAS Bottom Side

1. Mounting Holes
2. SMARC Connector

3.3.5 Processor (CPU)

The Intel Atom®/Pentium®/Celeron® 7xxx processor family is the base for the SMARC-sXAS.

		x7211RE	x7213RE	x7433RE	x7833RE
TDP		6W	9W	9W	12W
Cores		2		4	8
CPU	**Base**	1.0GHz	2.0GHz	1.5GHz	1.3GHz
	1C Turbo	3.2GHz	3.4GHz	3.4GHz	3.6GHz
	MC Turbo	2.9GHz	2.9GHz	2.7GHz	3.0GHz
GPU	**EU**	16EU		32EU	
	Base	400MHz	600MHz	600MHz	800MHz
	Turbo	1.0GHz	1.0GHz	1.0GHz	1.2GHz
ECC		Yes-In Band			
TCC RealTime		Yes			
Use Condition		Embedded / Industrial			

Table 7: Atom®/Pentium®/Celeron® 7xxx processor family

When RE-Series is used as Embedded use condition DTR = +- 90°C
For use as Industrial use condition turbo needs to be disabled – DTR = +- 110°C

Intel® DTR (Dynamic Temperature Range)

For this processor family the Dynamic Temperature Range (DTR) behavior applies. DTR is the temperature range the processor can operate in. The temperature range starts with the temperature of the processor (Tj = junction temperature) at boot time and can transition to a lower and/or higher temperature within the Tj min and Tj max limits.

E.g.: Tj min = -40°, the Tj max = 100°C and the DTR = +-90°C
TBoot = -40°C: the processor can operate from -40°C up to + 50°C
TBoot = -20°C: the processor can operate from -40°C up to + 70°C
TBoot = +20°C: the processor can operate from -40°C up to + 100°C

A Tj outside of the DTR range requires a cold reset but is not enforced by the hardware.

The behavior is described in Intel whitepaper 814861 as DTR = Dynamic Temperature Range. Please contact JUMPtec Support for further information.

CPU Use Condition	Industrial	Embedded
CPU Tjunction Min.	-40ºC	0°C
Max.	TBoot + 110ºC	TBoot + 70ºC
DTR (Hot to Cold Transition)	TBoot - 110ºC	TBoot - 70ºC

Table 8: DTR temperatures

In Industrial use condition, the following design recommendations must be in place for the entire duration of the product's operating lifetime to meet Intel's goals.

(Activity Factor (AF) is defined as the percentage of time that the interface signals are switching while the processor is active (in an S0 state) across the entire use condition duration.)

- The VCCANA power rail must be implemented in FIVR Mode. Implementing VCCANA in MBVR (Motherboard Voltage Regulator) Mode is not allowed.
  - HW is already prepared for FIVR mode
  - VCCANA FIVR Mode must also be enabled using the following soft strap: CPU Straps ⇒ CPU Straps ⇒ VCCANA VR Location = VCCANA is CPU FIVR
- The CPU & GPU Intel® Turbo Boost Technology 2.0 features should be disabled by the system BIOS, so the maximum frequency is limited to the HFM value.
- For the eMMC & TCSS interfaces, two design recommendation options are listed. Only one out of two of these options should be implemented:
  - Reduced Activity Factor
  - Reduced Freq

For further details please get in contact with JUMPtec Support.

3.3.6 Plattform Controller Hub (PCH)

The Atom®/Pentium®/Celeron® 7xxx processor family provides an On-Package PCH.

3.3.7 System Memory

The SMARC-sXAS supports up to 16 GByte LPDDR5 memory down (4800MT/s). The Intel Atom x7000RE and x7000E processor series supports in-band ECC.

3.3.8 HSIO Mapping

The integrated SoC PCH supports 9x HSIO lanes, which can be configured as PCIe Gen 3.0 lanes with a max of 5 RPC (Root Port Controller). Partially the HSIOs are multi-pupose and can be alternatively configured as USB3.2 Gen2 or SATA.

HSIO Lane	0	1	2	3	6	8	9	10	11
Default	PCIe	PCIe	PCIe	PCIe	GbE 1	PCIe	PCIe	SATA #0	SATA #1
SMARC Connector	PCIe #A	PCIe #B	PCIe #C	PCIe #D Optional USB#2	GbE1	GbE0 via i226	N.C.	SATA #0	N.C.

Table 9: HSIO Mapping

3.4 Interfaces

3.4.1 PCIe

The SMARC-sXAS supports up to four high-speed PCI Express 3.0 lanes PCIe [0-3], allowing for the connection of up to four separate external PCIe devices. The default PCIe configuration is (4 x1) with options for (1 x2 + 2 x1), (2 x2) and (1 x4).

SMARC Connector	**HSIO Lane**	**HSIO Port**	**Supported Lane Config**			
PCIE_A	0	PCIE 1 #1	x1	x2	x2	x4
PCIE_B	1	PCIE 1 #2	x1			
PCIE_C	2	PCIE 1 #3	x1	x1	x2	
PCIE_D	4	PCIE 1 #4	x1	x1		

Table 10: PCI Express

3.4.2 USB

The SMARC-sXAS provides one (optional two) USB 3.2 (10.0 Gb/S) SuperSpeed port(s) backwards compatible with USB 2.0 and six dedicated USB 2.0 ports.

USB 3.2

SMARC Connector	CPU	Description
USB2_SS	TCP1	USB-C Port used as 3.2 Gen2 (10Gb/s) to SMARC

Table 11: USB 3.2

USB 2.0

SMARC Connector	PCH USB Port	Description
USB0	USB2 1	-
USB1	USB2 2	-
USB2	USB2 6	TCP1 has to be paired with PCH USB2 Port 1, 2, 5 or 6.
USB3	USB2 3	-
USB4	USB2 4	-
USB5	USB2 5	-

Table 12: USB 2.0

USB 2.0 Client Mode

The USB subsystem also supports Dual Role Capability. The xHCI is paired with a standalone eXtensible Device Controller Interface (xDCI) to provide dual role functionality. The xDCI can be mapped to any of the USB ports, but there is only one endpoint supported. As SMARC-sXAS does not have an onboard Type-C PD controller, it supports static USB2.0 device mode only (No USB3.0 support due to the limitation by fixed USB_ID in software).

It does not support changing dynamically between host mode and device mode.
A BIOS settings change in setup menu and restart is required.

When designing the carrier board consider the speed of the USB 3.2 Gen2 (10 Gb/s).
JUMPtec recommends using a retimer/redriver on the carrier.

3.4.3 SATA 3.0

The SMARC-sXAS provides one SATA III 6Gb/s port.

SMARC Connector	HSIO Lane	HSIO Port	Description
SATA0	10	SATA 0	SATA 6Gb/s to SMARC

Table 13: SATA ports

3.4.4 Graphics Interfaces

The processor graphics are based on the Generation 12 graphics core architecture. The Gen 12 architecture supports up to 32 Execution Units (EUs), depending on the processor SKU. AML processor supports three simultaneous displays (Pipes A, B, C).

Processor	SMARC Port	
DDIA	LVDS	eDP (option)
DDIB	HDMI (optional DP++)	
TCP0	DP++	

Table 14: Graphic Interfaces

3.4.5 Audio Interface

HDA signals will passed through directly to SMARC.

SMARC Connector	PCH Pin	Description
HDA_RST#	HDA_RST#	
HDA_SYNC	HDA_SYNC	
HDA_CLK	HDA_BCLK	24.0 MHz clock to external codec
HDA_SDO	HDA_SDO	
HDA_SDI	HDA_SDI0	

Table 15: HDA

3.4.6 UART Interfaces

SMARC-SXAS support four serial ports. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

- Two UARTs provided from Embedded Controller
- Two UARTs provided by CPU

SMARC Signal	CPU Pin	Embedded Controller Pin
SER0_TX	-	GPIO104/UART0_TX
SER0_RX	-	GPIO105/UART0_RX
SER0_RTS#	-	GPIO144/UART0_RTS#
SER0_CTS#	-	GPIO143/UART0_CTS#
SER1_TX	-	GPIO170/UART1_TX
SER1_RX	-	GPIO171/UART1_RX
SER2_TX	GPP_H11/UART0_TXD	-
SER2_RX	GPP_H10/UART0_RXD	-
SER2_RTS#	GPP_H12/UART0_RTS#	-
SER2_CTS#	GPP_H13/UART0_CTS#	-

SMARC Signal	CPU Pin	Embedded Controller Pin
SER3_TX	GPP_D18/UART1_TXD	-
SER3_RX	GPP_D17/UART1_RXD	-

Table 16: UART Serial Ports

3.4.7 Boot SPI Interface

The Serial Peripheral Interface (SPI) bus is a synchronous serial data link where devices communicate in master/slave mode and the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

The SPI interface may only be used with a SPI Flash device to boot from the external BIOS on the carrier board.

The SPI Flash chip stores the BIOS to be booted. The SMARC-sXAS supports SPI boot from the 32 MByte SPI Flash chip on the board and an external 32 MByte SPI Flash chip on the carrier board.

The SPI flash chip on the carrier is required to be 32MByte (256MBit).

The module’s SPI voltage is 1.8V. Booting takes place either from the on-module SPI Flash chip or the external SPI Flash chip on the carrier board.

3.4.8 General Purpose SPI (GSPI) / eSPI

On SMARC connector side the GSPI is shared with eSPI functionality. SXAS connects a general purpose SPI (GSPI) port that’s provided by the onboard embedded controller (KSC20) to those pins by default. For options please refer the table below.

So there’s only one ESPI slave (Embedded Controller / KSC20) enabled in the BIOS. If a second eSPI slave on the carrier should be enabled a BIOS as well as HW modification is necessary.

General purpose SPI is provided by the SMARC Eval Carrier eSPI connector (J47).

SMARC Pin	GSPI (KSC20) (default)	eSPI (PCH) (option 1)	GSPI (PCH) (optional 2)
ESPI_CS0# / SPI1_CS0#	GPIO024 / GSPI_CS#	ESPI_CS1# / GPP_A23	GPP_E10 / GSPI0_CS0#
ESPI_CS1# / SPI1_CS1#	GPIO022	-	-
ESPI_CK / SPI1_CK	GPIO023 / GSPI_CLK	ESPI_CLK / GPP_A9	GPP_E11 / GSPI0_CLK

SMARC Pin	GSPI (KSC20) (default)	eSPI (PCH) (option 1)	GSPI (PCH) (optional 2)
ESPI_IO_0 / SPI1_DO	GPIO245 / GSPI_IO0	ESPI_IO0 / GPP_A0	GPP_E12 / GSPI0_MISO
ESPI_IO_1 / SPI1_DIN	GPIO243 / GSPI_IO1	ESPI_IO1 / GPP_A1	GPP_E13 / GSPI0_MOSI
ESPI_IO_2 / -	-	ESPI_IO2 / GPP_A2	-
ESPI_IO_3 / -	-	ESPI_IO3 / GPP_A3	-
ESPI_ALERT0# / -	-	ESPI_ALERT1# / GPP_A6	-
ESPI_ALERT1# / -	-	-	-
ESPI_RESET / -	-	ESPI_RESET# / GPP_A10	-

Table 17: GSPI / eSPI

3.4.10 I2C

The SMARC-sXAS contains two I2C interfaces I2C_GP and I2C_PM capable and a default data rates of 100 kHz.

3.4.11 GPIO

The SMARC-sXAS offers 14 GPIOs, generated by the onboard embedded controller. Configuration can to be done by the OS driver.

SMARC Signal	KSC	Alternative Use
GPIO0	GPIO011	CAM0_PWR#
GPIO1	GPIO012	CAM1_PWR#
GPIO2	GPIO013	CAM0_RST#
GPIO3	GPIO014	CAM1_RST#
GPIO4	GPIO015	HDA_RST#
GPIO5	GPIO002	PWM_OUT#
GPIO6	GPIO052	TACHIN
GPIO7	GPIO053	-
GPIO8	GPIO054	-
GPIO9	GPIO064	-
GPIO10	GPIO100	-
GPIO11	GPIO130	-
GPIO12	GPIO131	-
GPIO13	GPIO222	-

Table 18: General Purpose IOs

Defaults in BIOS are GPIOs except HDA_RST#, PWM_OUT# and TACHIN.

3.4.12 SMB

The System Management Bus (SMBus) is a simple 2-wire bus for low-speed system management communication. The (On-Package) PCH controls the SMBus. It is not used onboard on the module, but routed to the SMARC connector. The SMBus address uses the LSB (Bit 0) for the direction of the device. Bit0 = 0 defines the write address Bit0 = 1 defines the read address

3.3.13 CAN Bus

The CAN BUS communication according to ISO 11898-1 (identical to the Bosch CAN Protocol Specification 2.0 part A, B) and according to ISO 11898-4 (Time-triggered Communication on CAN). The Can Bus controller supports communication according to CAN FD Protocol Specification 1.0. The CAN FD option can be used together with event-triggered CAN communication.

SMARC Connector	SoC Pin	Description
CAN0_TX	PSE_CAN0_TX	Can Port 0 transmit output
CAN0_RX	PSE_CAN0_RX	Can Port 0 Receive output
CAN1_TX	PSE_CAN1_TX	Not supported on SXAS
CAN1_RX	PSE_CAN1_RX	Not supported on SXAS

Table 19: CAN Bus

3.4.14 Ethernet

There are two Gigabit Ethernet options on the SMARC-sXAS. The Amston Lake includes one Gigabit Ethernet (GbE) Time-Sensitive Networking (TSN) controller that resides in PCH. The GbE-TSN controller can operate at multiple speeds (10/100/1000 & 2500 Mbps Serial Gigabit Media-Independent Interface (SGMII)) and in either full duplex or half duplex mode.

External PHY

SXAS supports the usage of Intel GPY115 (default) Phy for 1Gbps operation as well as Intel GPY215 (optional) for speeds up to 2.5Gbps. Both Phys are pin-to-pin compatible and attached to the AML SGMII interface (PSE GbE#0, HSIO lane 7). The PHY uses an external SPI flash to support field firmware update (FFU) and load customized FW images to, for example, adjust LED pin behavior. It has an onboard OTP where the default firmware is pre-programmed.

I226

One Intel Foxville I226-IT Ethernet Controller is connected to PCH HSIO Port 8 (PCIe #9).

3.4.15 MIPI CSI

SMARC 2.1 defines two MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/-). CSI1 up to four differential data lanes (CSI1_D[0:3]+/-).

Amston Lake supports MIPI CSI-2 V2.0 only (the control interface (referred as CCI) is always a

bidirectional control interface compatible with I2C standard).

SMARC Pin	Amston Lake
CSI0_RX[0:1]±	CSI_C_DP/N[0:1]
CSI0_CK±	CSI_C_CLK_P/N
I2C_CAM0_CK	GPP_H7 / I2C1_SCL
I2C_CAM0_DAT	GPP_H6 / I2C1_SDA
CAM0_PWR# / GPIO0	GPP_A21
CAM0_RST# / GPIO2	GPP_R6
CAM_MCK	GPP_H20 / IMGCLKOUT0

Table 20: CSI0

SMARC Pin	Amston Lake
CSI1_RX[0:3]±	CSI_B_DP/N[0:3]
CSI1_CK±	CSI_B_CLK_P/N
I2C_CAM1_CK	GPP_B17 / I2C5_SCL
I2C_CAM1_DAT	GPP_B16 / I2C5_SDA
CAM1_PWR# / GPIO1	GPP_A22
CAM1_RST# / GPIO3	GPP_R7

Table 21: CSI1

3.5 Features

3.5.1 ACPI Power States

ACPI enables the system to power down, save power when not required (suspend) and wake up when required (resume). ACPI controls the power states S0-S5, where S0 has the highest priority and S5 the lowest priority.

S0	Working state
S1	Sleep (typically not supported anymore)
S2	Deep Sleep (typically not supported anymore)
S3	Suspend-to-RAM
S4	Suspend-to-disk / Hibernate
S5	Soft-off state

Table 22: ACPI Power States Function

Not all ACPI defined power states are available.

The SMARC-sXAS supports ACPI 6.0 and the power states S0, S3, S4, S5. To power on from state S3, S4, S5 use: Power Button, Wake On LAN

3.5.2 Embedded Controller

The Embedded Controller (EC) together with the Power Sequence Controller (PSC) provides a broad set of functionality:

- power sequencing control
- monitoring the module's processor temperature, power supply voltages V_IN_VAR, VCC_5V_SBY, VCC_RTC
- monitoring and configuring the on-board and external fans
- acting as hub or super-IO for low speed interfaces such as UART, I2C/SMB, GP_SPI, GPIO
- supporting watchdog functions

The EC is accessible through the API in the Board Support Package.

3.5.3 Trusted Platform Module

The SMARC-sXAS supports the firmware TPM (fTPM) using the integrated TPM 2.0 capability of the Intel Platform Trusted Technology (Intel® PTT). On request a dicrete TPM chip can be offered which is directly connected to the dedicated SPI interface from the PCH.

3.5.4 Watchdog

The SMARC-sXAS supports an independently programmable dual-stage software watchdog timer. The watchdog functionality is accessible through the API of the Embedded Controller (EC) in the related Board Support Package. The watchdog is able to generate IRQ (SWI), SMI and SCI dependent on the implementation.

Please find more information about the watchdog implementation in the according API user guide for the EC implementation.

Time-out event	**Description**
No action	Stage is off and will be skipped
Reset	Restarts the module and starts a new POST and operating system
NMI	A non-maskable interrupt (NMI) is a computer processor interrupt that cannot be ignored by standard interrupt masking techniques in the system. It is used typically to signal attention for non-recoverable hardware errors.
SMI	A system management interrupt (SMI) makes the processor entering the system management mode (SMM). As such, specific BIOS code handles the interrupt. The current BIOS handler for the watchdog SMI currently does nothing. For special requirements, contact JUMPtec Support
SCI	A system control interrupt (SCI) is a OS-visible interrupt to be handled by the OS using AML code

Time-out event	Description
Delay	Might be necessary when an operating system must be started and the time for the first trigger pulse must be extended.

Table 23: Watchdog Events

3.5.5 RTC

The RTC keeps track of the current time accurately. The RTC's low power consumption means that the RTC can be powered from an alternative source of power enabling the RTC to continue to keep time while the primary source of power is off or unavailable. The RTC's battery voltage range is 2.0 V to 3.25 V. Typical RTC values are 3 V and less than 10 µA. If the module is powered by mains supply, the RTC voltage is generated by on-module regulators, to reduce RTC current draw. The SMARC-sXAS supports an internal RTC by default with the option for an external RTC on request such as a lithium cell or super cap on the carrier board.

Using the SMARC-sXAS without RTC battery voltage supply may result in improper behavior. Contact JUMPtec Support in case you plan a carrier design without RTC battery.

3.5.6 eMMC Flash Memory

The Embedded Multimedia Flash Card (eMMC) is eMMC 5.1 compatible. The standard eMMC Flash memory is TLC. On request eMMC pSLC can be offered. During the manufacturing process, Triple Level Cell (TLC) eMMC is reconfigured to act as pseudo Single Level Cell (pSLC) eMMC to provide improved reliability, endurance and performance. The module's eMMC flash memory supports up to 85 GByte pSLC or 256 GByte TLC.

Pseudo SLC (pSLC) memory is a reconfigured MLC/TLC eMMC.
MLC to pSLC: the capacity is half of a MLC memory.
TLC to pSLC: the capacity is a third of the TLC memory.

3.5.7 EEPROM

The embedded EEPROM (EeeP) is connected to I2C_GP bus from the CPLD and operates at 1.8 V. The EEEP address is A0h (8bit format). The EEPROM retains module parameter information, including the module serial number and data structure and conforms to the PICMG® EEEP Embedded EEPROM Specification.

3.5.8 Features on Request

For the SMARC-sXAS following optional features are available on request:

Optional Features (on request)	
Feature	**Description**
x7000E	CPU from x7000E processor series
LPDDR5	Memory down up to 16 GB
eMMC 5.1	Up to 256GB eMMC 5.1 Flash TLC technology - configuration as pSLC can be offered
TPM	Discrete TPM 2.0 chip
eDP	Support of eDP instead of LVDS
eSPI	Instead of LPC signals, eSPI signals are routed to the according pins of the SMARC connector
UART	2 UART serial RX/TX ports from SOC (PCIe based, non-legacy) instead of Embedded Controller
GP-SPI	Signals routed to SPI pins of SMARC connector
MIPI-CSI	Connecting flatfoil
USB 3.2	2nd USB 3.2 instead of PCIe#3

Table 24: Features on Request

3.6 Electrical Specification

The SMARC-sXAS powers on by connecting to a carrier board via the SMARC connector. Before connecting the module to the carrier board, ensure that the carrier board is switch off and disconnected from the main power supply at the time of connection. Failure to disconnect the main power supply from the carrier board could result in personal injury and damage to the module and/or carrier board. The SMARC connector pins on the module limits the amount of power received. The module receives power on the ten VDD-IN pins that operate over the VDD-IN range of 4.75 VDC to 5.25 VDC. The current rating of each connector pin is 0.5 A and for ten pins 5 A (0.5 A x 10).

The SMARC-sXAS powers on by connecting to the carrier board using the Interface connector. Before connecting the module to the carrier board’s corresponding connector, ensure that the carrier board is switch off and disconnected from the main power supply. Failure to disconnect the main power supply could result in personal injury and damage to the module and/or carrier board.

Observe that only trained personnel aware of the associated dangers connect the module, within an access controlled ESD-safe workplace.

Supply Voltage (VDD-IN)	5V only! No Widerange

RTC	2.3 VDC to 3.25 VDC
Input Current	5 A max. on all ten VDD_IN pins (0.5 A max. per pin)

Table 25: Power Supply Voltage Requirements

Only connect to an external power supply delivering the specified input rating and complying with the requirements of Safety Extra Low Voltage (SELV) and Limited Power Source (LPS) of UL/IEC 60950-1 or (PS2) of UL/IEC 62368-1.

To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN 62368-1.

If an under voltage (brownout) condition occurs the used power supply must remain in the “off state” long enough to allow internal voltages to discharge sufficiently. Failure to observe this “off state” may mean that parts of the product or peripherals work incorrectly or suffer a reduction of MTBF. The minimum “off state”, to allow internal voltages to discharge sufficiently, is dependent on the power supply and additional electrical factors. To determine the required “off state”, each case must be considered individually. For more information, contact JUMPtec Support.

3.7 Thermal Management

3.7.1 Heatspreader

A heatspreader plate assembly is available from JUMPtec for the SMARC-sXAS. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a SMARC-standard thermal interface to use with a heat sink or external cooling devices. External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according to the module specification:

- 60°C for commercial grade modules
- 85°C for industrial temperature grade modules (E2/XT)

Documentation and CAD drawing of the heatspreader and cooling solutions are available on request from JUMPtec’s Customer Section.

JUMPtec recommends the use of thermal interfaces between the heatspreader plate and the major heat-generating components. About 80 % of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution. Heatspreaders are available as an accessory for both commercial and industrial temperature grades.

3.7.2 Thermal Sensors

The SMARC-sXAS uses an on-chip thermal sensors located within the CPU to measure the CPU temperature, and a thermal sensor close to the Hardware monitor chip to measure the module temperature.

3.7.3 Fan Connector

The analog output voltage on this connector is generated via a discrete linear voltage regulator from the PWM signal of the HWM. It is clipped at 12 V (+/- 10 %) across the whole input range of the module to prevent FAN damage at higher voltages. FAN signals are connected to a 3-pin-connector. The maximum supply current to the fan is 350mA for an input voltage of 5.0V.

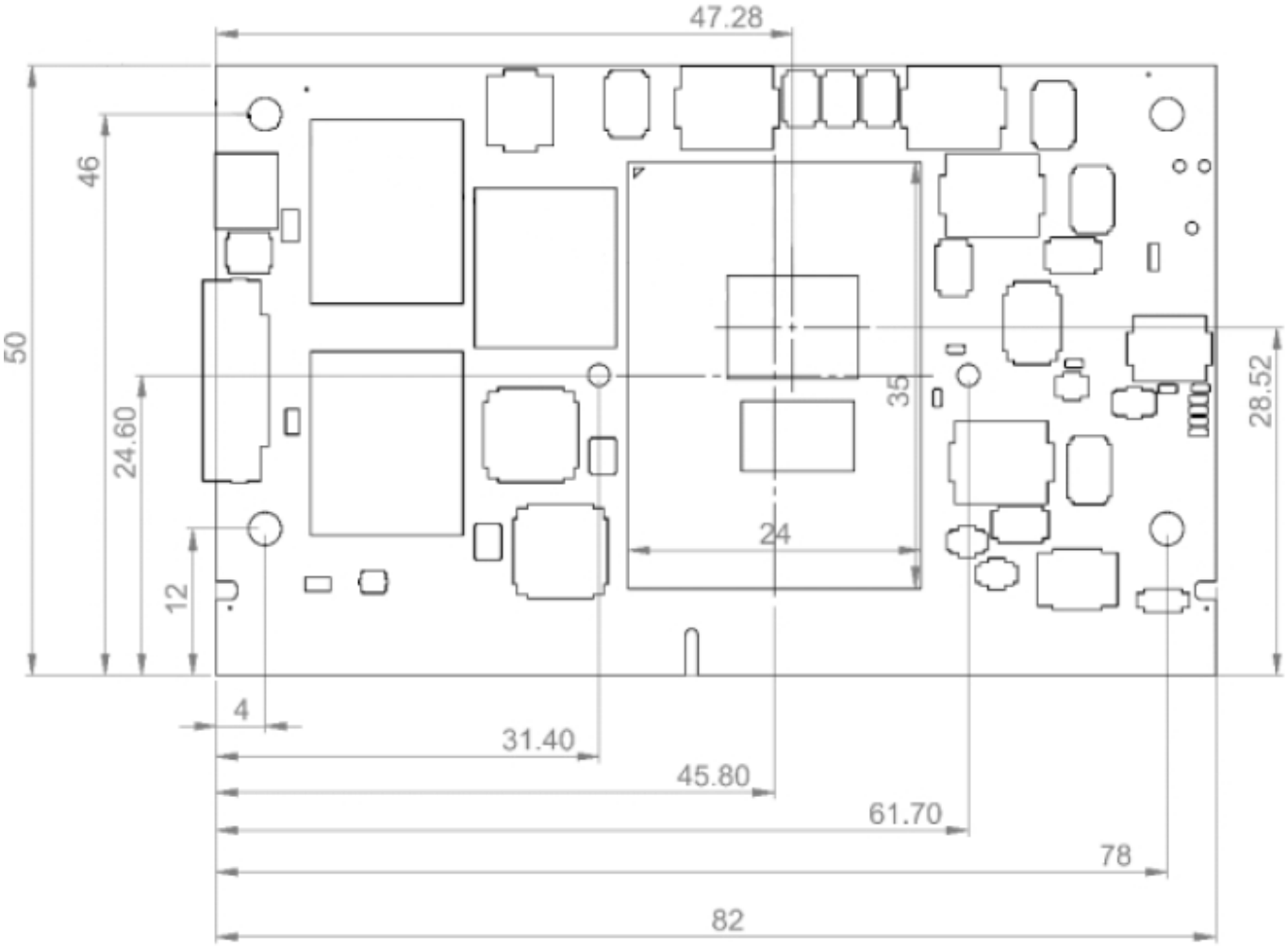
Connector Pin	Description
1	FAN_TACH_IN#
2	V_FAN
3	GND

Table 26: Fan Connector

3.8 Mechanical Specification

The SMARC short module form factor is 82 mm x 50 mm and includes four mounting holes per SMARC specification. There are two additional holes to enable the attachment of a thermal device such as a heatsink/heatspreader. The total height of the SMARC-sXAS module depends on the height of the implemented cooling solution.

3.8.1 Mechanical Drawings



3.9 Environmental Specification

The standard versions of the SMARC-sXAS supports industrial temperature grade only.

Environmental		**Description**
Industrial Grade (E2)	Operating	-40°C to +85°C (-40°F to 185°F)
	Non-operating	-40°C to +85°C (-40°F to 185°F)
Relative Humidity		93 % @40°C, non-condensing
Shock (according to IEC 60068-2-27)		Non-operating shock test (half-sinusoidal, 11ms, 15g)
Vibration (according to IEC 60068-2-6)		Non-operating vibration (sinusoidal, 10 Hz to 2000 Hz, +/- 0.15 mm, 2 g)

Table 27: Environmental Specification

3.10 Compliance

The SMARC-sXAS complies with the following or the latest status thereof. If modified, the prerequisites for specific approvals may no longer apply. For more information, contact JUMPtec Support.

Europe - CE Mark	
Directives	**2014/30/EU**: Electromagnetic Compatibility **2014/35/EU**: Low Voltage **2011/65/EU**: RoHS II **2001/95/EC**: General Product Safety
EMC	**EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 28: Compliance CE Mark

USA/Canada	
Safety	**UL 62368-1 & CSA C22.2 No. 62368-1 (Component Recognition)**: Audio/video, information and communication technology equipment - Part 1: Safety requirements Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements. **UL listings**: AZOT2.E547070 AZOT8.E547070
UK CA Mark	
EMC	**BS EN 55032 Class B**: Electromagnetic compatibility of multimedia equipment - Emission Requirements Class A **BS EN 61000-6-2**: Electromagnetic compatibility (EMC) Part 6-2: Generic standards - Immunity standard for industrial environments
Safety	**BS EN 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements
CB scheme (For International Certifications)	
Safety	**IEC 62368-1**: Audio/video, information and communication technology equipment - Part 1: Safety requirements

Table 29: Country Compliance

If the product is modified, the prerequisites for specific approvals may no longer apply.

JUMPtec is not responsible for any radio television interference caused by unauthorized modifications of the delivered product or the substitution or attachment of connecting cables and equipment other than those specified by JUMPtec. The correction of interference caused by unauthorized modification, substitution or attachment is the user's responsibility.

3.11 MTBF

The MTBF (Mean Time Before Failure) values were calculated using a combination of the manufacturer's test data (if available) and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.
The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment. This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned-in. Other environmental stresses (such as extreme altitude, vibration, salt-water exposure) lower MTBF values.

	MTBF Value @40°C	**Part Number**
MTBF (hours)	879.034	51018-3285R2-9EVL

Table 30: MTBF

The MTBF estimated value above assumes no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for and needs to be considered separately. Battery life depends on both temperature and operating conditions. When the module is connected to external power, the only battery drain is from leakage paths.

4. Pin Definitions

The following sections provide pin definitions and detailed description of all on-board connectors. The connector definitions follow the following notation.

	Description	
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.	
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.	
Type	AI	Analog Input
	AO	Analog Output
	I	Input, TTL compatible if nothing else stated
	IO	Input / Output, TTL compatible if nothing else stated
	IOT	Bi-directional tristate IO pin.
	IS	Schmitt-trigger input, TTL compatible.
	IOC	Input / open-collector Output, TTL compatible
	IOD	Input / Output, CMOS level Schmitt-triggered (Open drain output)
	NC	Not Connected
	O	Output, TTL compatible
	OC	Output, open-collector or open-drain, TTL compatible
	OT	Output with tri-state capability, TTL compatible
	LVDS	Low Voltage Differential Signal
	PWR	Power supply or ground reference pins
	Ioh	Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated).
	Iol	Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated)
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins	
Note	Special remarks concerning the signal	
Designation	Type and number of item described	

Table 31: Connector Definitions

4.1.1 Pinout of SMARC Connector (Top Side)

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P1	SMB_ALERT#	SMBus Alert# (Interrupt) Signal	I OD CMOS	1.8 to 5V Standby	PU 2.2K (3.3V)	—
P2	GND	Power Ground	PWR GND	—	—	—
P3	CSI1_CK+	CSI1 differential clock input (point to point)	I D-PHY	Runtime	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P4	CSI1_CK-	CSI1 differential clock input (point to point)	I D-PHY	Runtime	—	—
P5	GBE1_SDP	IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	I/O CMOS	3.3V Standby	PD 10K	GPY115 GPC2 pin connected by default optional connection to PCH TIME_SYNC0 possible
P6	GBE0_SDP	IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)	I/O CMOS	3.3V Standby	PD 10K	I226 SDP0 pin connected by default optional connection to PCH TIME_SYNC0 possible
P7	CSI1_RX0+	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P8	CSI1_RX0-	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P9	GND	Power Ground	PWR GND	—	—	—
P10	CSI1_RX1+	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P11	CSI1_RX1-	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P12	GND	Power Ground	PWR GND	—	—	—
P13	CSI1_RX2+	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P14	CSI1_RX2-	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P15	GND	Power Ground	PWR GND	—	—	—
P16	CSI1_RX3+	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P17	CSI1_RX3-	CSI1 differential input (point to point)	I D-PHY / I M-PHY	Runtime	—	—
P18	GND	Power Ground	PWR GND	—	—	—
P19	GBE0_MDI3-	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	Standby	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
P20	GBE0_MDI3+		I/O GBE MDI	Standby	—	
P21	GBE0_LINK_MID#	Link Speed Indication LED for GBE0 lower link speed	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current
P22	GBE0_LINK_MAX#	Link Speed Indication LED for GBE0 maximum link speed	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current
P23	GBE0_MDI2-	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	—	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
P24	GBE0_MDI2+		I/O GBE MDI	—	—	
P25	GBE0_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P26	GBE0_MDI1-	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	—	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
P27	GBE0_MDI1+		I/O GBE MDI	—	—	
P28	GBE0_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic	Analog	0 to 3.3V max	100nF cap	if required by the Module GBE PHY
P29	GBE0_MDI0-	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	—	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
P30	GBE0_MDI0+		I/O GBE MDI	—	—	
P31	SPI0_CS1#	SPI0 Master Chip Select 1	O CMOS	1.8V Standby	PU 10K	—
P32	GND	Power Ground	PWR GND	—	—	—
P33	SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I OD CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P34	SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P35	SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	I OD CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P36	SDIO_CK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P37	SDIO_PWR_EN	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS	3.3V Runtime	nc	Not supported on SXAS
P38	GND	Power Ground	PWR GND	—	—	—
P39	SDIO_D0	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P40	SDIO_D1	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P41	SDIO_D2	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P42	SDIO_D3	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS	1.8V or 3.3V Runtime	nc	Not supported on SXAS
P43	SPI0_CS0#	SPI0 Master Chip Select 0	O CMOS	1.8V Standby	PU 10K	This signal can be used to select Carrier SPI as boot device
P44	SPI0_CK	SPI0 Clock	O CMOS	1.8V Standby	PD 100K	—
P45	SPI0_DIN	SPI0 Master input / Slave output	I CMOS	1.8V Standby	—	also referred to as MISO
P46	SPI0_DO	SPI0 Master output / Slave input	O CMOS	1.8V Standby	PU 4.7K	also referred to as MOSI
P47	GND	Power Ground	PWR GND	—	—	—
P48	SATA_TX+	Serial ATA Channel 0 Transmit Output Differential Pair	O SATA	Runtime	—	series AC coupled on Module (10nF)
P49	SATA_TX-		O SATA	Runtime	—	
P50	GND	Power Ground	PWR GND	—	—	—
P51	SATA_RX+	Serial ATA Channel 0 Receive Input Differential Pair	I SATA	Runtime	—	series AC coupled on Module (10nF)
P52	SATA_RX-		I SATA	Runtime	—	
P53	GND	Power Ground	PWR GND	—	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P54	ESPI_CS0# /	ESPI1 Master Chip Select 0	O CMOS	1.8V Standby	—	PCH ESPI_CS1#
	SPI1_CS0# /	SPI1 Master Chip Select 0	O CMOS	1.8V Standby	—	See corresponding chapter for more details about GSPI/eSPI pin sharing
	QSPI_CS0#	QSPI Master Chip Select 0	O CMOS	1.8V Standby	—	Not supported on SXAS
P55	ESPI_CS1# /	ESPI1 Master Chip Select 1	O CMOS	1.8V Standby	nc	Not supported on SXAS
	SPI1_CS1# /	SPI1 Master Chip Select 1	O CMOS	1.8V Standby	—	—
	QSPI_CS1#	QSPI Master Chip Select 1	O CMOS	1.8V Standby	—	Not supported on SXAS
P56	ESPI_CK /	ESPI Master Clock Output	O CMOS	1.8V Standby	—	—
	SPI1_CK /	SPI1 Clock	O CMOS	1.8V Standby	—	See corresponding chapter for more details about GSPI/eSPI pin sharing
	QSPI_CK	QSPI Clock	O CMOS	1.8V Standby	—	Not supported on SXAS
P57	ESPI_IO_1 /	ESPI Master Data Input / Output	I/O CMOS	1.8V Standby	—	—
	SPI1_DIN /	SPI1 Master input / Slave output	I CMOS	1.8V Standby	—	also referred to as MISO
	QSPI_IO_1	QSPI Data input / output	I/O CMOS	1.8V Standby	—	Not supported on SXAS
P58	ESPI_IO_0 /	ESPI Master Data Input / Output	I/O CMOS	1.8V Standby	—	—
	SPI1_DO /	SPI1 Master output / Slave input	O CMOS	1.8V Standby	—	also referred to as MOSI
	QSPI_IO_0	QSPI Data input / output	I/O CMOS	1.8V Standby	—	Not supported on SXAS
P59	GND	Power Ground	PWR GND	—	—	—
P60	USB0+	USB Differential Data Pairs for Port 0	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
P61	USB0-		I/O USB	USB		—
P62	USB0_EN_OC#	USB Over-Current Sense for Port 0	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P63	USB0_VBUS_DET	USB Port 0 Host Power Detection	I USB VBUS 5V	USB VBUS 5V	nc	When this Port is used as a device it can be connected to a USB client port VBUS pin.
P64	USB0_OTG_ID	Input Pin to Announce OTG Device Insertion on USB 2.0 Port	—	—	nc	Resistor value to ground according to USB specification
P65	USB1+	USB Differential Data Pairs for Port 1	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
P66	USB1-		I/O USB	USB		—
P67	USB1_EN_OC#	USB Over-Current Sense for Port 1	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB1 power. Pulled low by Carrier OD driver to indicate over- current situation.
P68	GND	Power Ground	PWR GND	—	—	—
P69	USB2+	USB Differential Data Pairs for Port 2	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
P70	USB2-		I/O USB	USB		—
P71	USB2_EN_OC#	USB Over-Current Sense for Port 2	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB2 power. Pulled low by Carrier OD driver to indicate over- current situation.
P72	RSVD	—	—	—	—	—
P73	RSVD	—	—	—	—	—
P74	USB3_EN_OC#	USB Over-Current Sense for Port 3	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB3 power. Pulled low by Carrier OD driver to indicate over- current situation
P75	PCIE_A_RST#	PCIe Port A reset output	O CMOS	3.3V Runtime	PD 10K	Copy of PCH PLTRST#
P76	USB4_EN_OC#	USB Over-Current Sense for Port 4	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB4 power. Pulled low by Carrier OD driver to indicate over- current situation.

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P77	PCIE_B_CKREQ#	PCIe Port B clock request	IO OD CMOS	3.3V Runtime	PU10K	Can be used for power saving mode on PCIe.
P78	PCIE_A_CKREQ#	PCIe Port A clock request	IO OD CMOS	3.3V Runtime	PU10K	Can be used for power saving mode on PCIe.
P79	GND	Power Ground	PWR GND	—	—	—
P80	PCIE_C_REFCK+	Differential PCIe Link C reference clock output	O PCIE	Runtime	—	f = 100MHz
P81	PCIE_C_REFCK-		O PCIE	Runtime	—	
P82	GND	Power Ground	PWR GND	—	—	—
P83	PCIE_A_REFCK+	Differential PCIe Link A reference clock output	O PCIE	Runtime	—	f = 100MHz
P84	PCIE_A_REFCK-		O PCIE	Runtime	—	
P85	GND	Power Ground	PWR GND	—	—	—
P86	PCIE_A_RX+	Differential PCIe link A receive data pair	I PCIE	Runtime	—	series AC coupled off Module 75-265nF depending on PCIe generation
P87	PCIE_A_RX-		I PCIE	Runtime	—	
P88	GND	Power Ground	PWR GND	—	—	—
P89	PCIE_A_TX+	Differential PCIe link A transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
P90	PCIE_A_TX-		O PCIE	Runtime	—	
P91	GND	Power Ground	PWR GND	—	—	—
P92	HDMI_D2+ /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE0+	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
P93	HDMI_D2- /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE0-	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
P94	GND	Power Ground	PWR GND	—	—	—
P95	HDMI_D1+ /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE1+	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P96	HDMI_D1- /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE1-	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
P97	GND	Power Ground	PWR GND	—	—	—
P98	HDMI_D0+ /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE2+	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
P99	HDMI_D0- /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	Runtime	—	—
	DP1_LANE2-	Secondary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
P100	GND	Power Ground	PWR GND	—	—	—
P101	HDMI_CK+ /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	—	—	AC coupled off Module
	DP1_LANE3+	Secondary DP Port Differential Pair Data Lines	O DP	—	—	AC coupled off Module 100nF DC blocking capacitors shall be placed on the Carrier
P102	HDMI_CK- /	HDMI Port, Differential Pair Data Lines	O TMDS HDMI	—	—	AC coupled off Module
	DP1_LANE3-	Secondary DP Port Differential Pair Data Lines	O DP	—	—	AC coupled off Module 100nF DC blocking capacitors shall be placed on the Carrier
P103	GND	Power Ground	PWR GND	—	—	—
P104	HDMI_HPD /	HDMI Hot Plug Active High Detection Signal that Serves as an Interrupt Request	I CMOS	1.8V Runtime	PD 1M	Module tolerates high level in standby mode.
	DP1_HPD	DP Hot Plug Detect Input	I CMOS	1.8V Runtime	PD 1M	

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P105	HDMI_CTRL_CK /	I2C_CLK Line Dedicated to HDMI	I/O OD	1.8V Runtime	PU 100K	Level shifter FET and 5V PU resistor shall be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board
	DP1_AUX+	Secondary DP Port. Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V Runtime	PD 100K	If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100K PD. If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100K PU. Stronger pull-up is demanded to the Carrier Board.
P106	HDMI_CTRL_DAT /	I2C_DAT Line Dedicated to HDMI	I/O OD	1.8V Runtime	PU 100K	Level shifter FET and 5V PU resistor shall be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board
	DP1_AUX-	Secondary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V Runtime	PU 100K	If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100K PU. If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100K PU. Stronger pull-up is demanded to the Carrier Board.

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P107	DP1_AUX_SEL	Strapping Signal to Enable Either HDMI or DP Output	I CMOS	1.8V Runtime	PD 1M	Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI mode. Module tolerates high level in stand-by mode. Should be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.
P108	GPIO0	GPIO Pin 0 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO0 / CAM0 function switchable in BIOS setup.
	CAM0_PWR#	Camera 0 Power Enable	O CMOS	1.8V Runtime	PU 499K	GPIO0 configured by default
P109	GPIO1	GPIO Pin 1 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO1 / CAM1 function switchable in BIOS setup.
	CAM1_PWR#	Camera 1 Power Enable	O CMOS	1.8V Runtime	PU 499K	GPIO1 configured by default
P110	GPIO2	GPIO Pin 2 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO2 / CAM0 function switchable in BIOS setup.
	CAM0_RST#	Camera 0 reset	O CMOS	1.8V Runtime	PU 499K	GPIO2 configured by default
P111	GPIO3	GPIO Pin 3 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO3 / CAM1 function switchable in BIOS setup.
	CAM1_RST#	Camera 1 reset	O CMOS	1.8V Runtime	PU 499K	GPIO3 configured by default
P112	GPIO4	GPIO Pin 4 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO4 / HAD_RST# function switchable in BIOS setup.
	HDA_RST#	High Definition Audio Reset Output to Codec	O CMOS	1.8V Runtime	PU 499K	HDA_RST# configured by default

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P113	GPIO5	GPIO Pin 5 Preferred Output	I/O CMOS	1.8V Runtime	PU 499K	GPIO5 / PWM_OUT function switchable in BIOS setup.
	PWM_OUT	Fan Speed Control	O CMOS	1.8V Runtime	PU 499K	PWM_OUT configured by default
P114	GPIO6	GPIO Pin 6 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	GPIO6 / TACHIN function switchable in BIOS setup.
	TACHIN	Fan Tachometer Input	I CMOS	1.8V Runtime	PU 499K	TACHIN configured by default
P115	GPIO7	GPIO Pin 7 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
P116	GPIO8	GPIO Pin 8 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
P117	GPIO9	GPIO Pin 9 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
P118	GPIO10	GPIO Pin 10 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
P119	GPIO11	GPIO Pin 11 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
P120	GND	Power Ground	PWR GND	—	—	—
P121	I2C_PM_CK	Power management I2C bus CLK	I/O OD CMOS	1.8V Standby	PU 2.2K	Connected to PCH SMB on SXAS.
P122	I2C_PM_DAT	Power management I2C bus CLK	I/O OD CMOS	1.8V Standby	PU 2.2K	Could be switched to KSC20 I2C_GP via BIOS setup option.
P123	BOOT_SEL0#	Input straps determine the Module boot device	I OD CMOS	1.8V Standby	PU 10K	Driven by OD on Carrier See corresponding chapter for more details about the boot device selection.
P124	BOOT_SEL1#		I OD CMOS	1.8V Standby	PU 10K	
P125	BOOT_SEL2#		I OD CMOS	1.8V Standby	PU 10K	
P126	RESET_OUT#	General purpose reset output to Carrier Board.	O CMOS	1.8V Standby	PD 10K	Copy of PCH PLTRST#

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P127	RESET_IN#	Reset input from Carrier Board	I OD CMOS	1.8V to 5V Standby	PU 10K	Carrier drives low to force a Module reset, floats the line otherwise. This signal is level triggered during bootup to allow to stop booting of the module. After bootup it is an edge triggered signal.
P128	POWER_BTN#	Power-button input from Carrier Board	I OD CMOS	1.8V to 5V Standby	PU 10K	—
P129	SER0_TX	Asynchronous Serial Data Output Port 0	O CMOS	1.8V Runtime	—	—
P130	SER0_RX	Asynchronous Serial Data Input Port 0	I CMOS	1.8V Runtime	PU 100K	—
P131	SER0_RTS#	Request to Send Handshake Line for Port 0	O CMOS	1.8V Runtime	—	—
P132	SER0_CTS#	Clear to Send Handshake Line for Port 0	I CMOS	1.8V Runtime	PU 100K	—
P133	GND	Power Ground	PWR GND	—	—	—
P134	SER1_TX	Asynchronous Serial Data Output Port 1	O CMOS	1.8V Runtime	—	—
P135	SER1_RX	Asynchronous Serial Data Input Port 1	I CMOS	1.8V Runtime	PU 100K	—
P136	SER2_TX	Asynchronous Serial Data Output Port 2	O CMOS	1.8V Runtime	—	—
P137	SER2_RX	Asynchronous Serial Data Input Port 2	I CMOS	1.8V Runtime	PU 100K	—
P138	SER2_RTS#	Request to Send Handshake Line for Port 2	O CMOS	1.8V Runtime	—	—
P139	SER2_CTS#	Clear to Send Handshake Line for Port 2	I CMOS	1.8V Runtime	PU 100K	—
P140	SER3_TX	Asynchronous Serial Data Output Port 3	O CMOS	1.8V Runtime	—	—
P141	SER3_RX	Asynchronous Serial Data Input Port 3	I CMOS	1.8V Runtime	PU 100K	—
P142	GND	Power Ground	PWR GND	—	—	—
P143	CAN0_TX	CAN Port 0 Transmit Output	O CMOS	1.8V Runtime	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
P144	CAN0_RX	CAN Port 0 Receive Input	I CMOS	1.8V Runtime	—	—
P145	CAN1_TX	CAN Port 1 Transmit Output	O CMOS	1.8V Runtime	nc	Not supported on SXAS
P146	CAN1_RX	CAN Port1 Receive Input	I CMOS	1.8V Runtime	nc	Not supported on SXAS
P147	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	SXAS supports fixed 5V supply only
P148	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P149	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P150	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P151	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P152	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P153	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P154	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P155	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	
P156	VDD_IN	Module power input voltage	Analog	4.75V to 5.25V	—	

Table 32: SMARC Connector top side

4.1.2 Pinout of SMARC Connector (Bottom Side)

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S1	CSI1_TX+ /	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS /	1.8V Runtime	PU 2.2K	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+/- diff. pair no PU required SXAS supports CSI 2.0 mode (CAM I2C) only.
	I2C_CAM1_CK		O M-PHY	Runtime	—	
S2	CSI1_TX- /	I2C data for serial camera data support link or differential data lane	I/O OD CMOS /	1.8V Runtime /	PU 2.2K /	
	I2C_CAM1_DAT		O M-PHY	Runtime	—	
S3	GND	Power Ground	PWR GND	—	—	—
S4	RSVD	—	—	—	nc	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S5	CSI0_TX+ /	I2C clock for serial camera data support link or differential data lane	I/O OD CMOS /	1.8V Runtime /	PU 2.2K /	MIPI-CSI 2.0 mode uses I2C_CAM1_CK MIPI-CSI 3.0 mode uses CSI1_TX+/- diff. pair no PU required SXAS supports CSI 2.0 mode (CAM I2C) only.
	I2C_CAM0_CK		O M-PHY	Runtime	—	
S6	CAM_MCK	Master clock output	O CMOS	1.8V Runtime	—	—
S7	CSI0_TX- /	I2C data for serial camera data support link or differential data lane	I/O OD CMOS /	1.8V Runtime /	PU 2.2K /	See pin S5
	I2C_CAM0_DAT		O M-PHY	Runtime	—	
S8	CSI0_CK+	CSI0 differential clock input (point to point)	I D-PHY	Runtime	—	—
S9	CSI0_CK-	CSI0 differential clock input (point to point)	I D-PHY	Runtime	—	—
S10	GND	Power Ground	PWR GND	—	—	—
S11	CSI0_RX0+	CSI0 differential input	I D-PHY / I M-PHY	Runtime	—	—
S12	CSI0_RX0-	CSI0 differential input	I D-PHY / I M-PHY	Runtime	—	—
S13	GND	Power Ground	PWR GND	—	—	—
S14	CSI0_RX1+	CSI0 differential input	I D-PHY / I M-PHY	Runtime	—	—
S15	CSI0_RX1-	CSI0 differential input	I D-PHY / I M-PHY	Runtime	—	—
S16	GND	Power Ground	PWR GND	—	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S17	GBE1_MDI0+	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	Standby	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
S18	GBE1_MDI0-		I/O GBE MDI	Standby	—	
S19	GBE1_LINK_MID#	Link Speed Indication LED for GBE1 lower link speed	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current
S20	GBE1_MDI1+	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	Standby	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
S21	GBE1_MDI1-		I/O GBE MDI	Standby	—	
S22	GBE1_LINK_MAX#	Link Speed Indication LED for GBE1 lower link speed	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current
S23	GBE1_MDI2+	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	Standby	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
S24	GBE1_MDI2-		I/O GBE MDI	Standby	—	
S25	GND	Power Ground	PWR GND	—	—	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S26	GBE1_MDI3+	Media Dependent Interface Differential Pairs for External Transformer	I/O GBE MDI	Standby	—	Carrier Series Termination: Magnetics Module appropriate for 10/100/1000 GBE transceivers Carrier Parallel Termination: Secondary side center tap terminations appropriate for Gigabit Ethernet implementations
S27	GBE1_MDI3-		I/O GBE MDI	Standby	—	
S28	GBE1_CTREF	Center-Tap Reference Voltage for Carrier Board Ethernet Magnetic	Analog	0 to 3.3V max	100nF cap	if required by the Module GBE PHY
S29	PCIE_D_TX+ /	Differential PCIe link D transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
	SERDES_0_TX+	Differential SERDES 0 Transmit Data Pair	O PCIE	Runtime	—	SERDES option not supported on SXAS
S30	PCIE_D_TX- /	Differential PCIe link D transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
	SERDES_0_TX-	Differential SERDES 0 Transmit Data Pair	O PCIE	Runtime	—	SERDES option not supported on SXAS
S31	GBE1_LINK_ACT#	Link / Activity Indication LED Driven Low on Link (10, 100 or 1000 Mbps) Blinks on Activity	O OD CMOS	3.3V Standby	—	able to sink up to 24mA Carrier LED current
S32	PCIE_D_RX+ /	Differential PCIe link D receive data pair	I PCIE	Runtime	—	Series AC coupled off Module 75-265nF depending on PCIe generation
	SERDES_0_RX+	Differential SERDES 0 Receive Data Pair	I PCIE	Runtime	—	SERDES option not supported on SXAS
S33	PCIE_D_RX- /	Differential PCIe link D receive data pair	I PCIE	Runtime	—	Series AC coupled off Module 75-265nF depending on PCIe generation
	SERDES_0_RX-	Differential SERDES 0 Receive Data Pair	I PCIE	Runtime	—	SERDES option not supported on SXAS
S34	GND	Power Ground	PWR GND	—	—	—
S35	USB4+	USB Differential Data Pairs for Port 4	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
S36	USB4-		I/O USB	USB		—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S37	USB3_VBUS_DET	USB Port 3 Host Power Detection	I USB VBUS 5V	USB VBUS 5V	nc	When this Port is used as a device it can be connected to a USB client port VBUS pin.
S38	AUDIO_MCK	Master Clock Output to I2S Codecs	O CMOS	1.8V Runtime	15ohm series	15ohm series termination on modules
S39	I2S0_LRCK	I2S0 Left & Right Synchronization Clock	I/O CMOS	1.8V Runtime	33ohm series	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S40	I2S0_SDOUT	I2S0 Digital Audio Output	O CMOS	1.8V Runtime	33ohm series	—
S41	I2S0_SDIN	I2S0 Digital Audio Input	I CMOS	1.8V Runtime	33ohm series	—
S42	I2S0_CK	I2S0 Digital Audio Clock	I/O CMOS	1.8V Runtime	33ohm series	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
S43	ESPI_ALERT0#	ESPI ALERT	I OD CMOS	1.8V Standby	PU in PCH	Connected to PCH ESPI_ALERT1# PCH ESPI_ALERT0# connected to module management controller (KSC20)
S44	ESPI_ALERT1#	ESPI ALERT	I OD CMOS	1.8V Standby	PU 4.7K	Not supported on SXAS
S45	MDIO_CLK	MDIO Signals to Configure Possible PHYs	O CMOS	1.8V Runtime	nc	Not supported on SXAS
S46	MDIO_DAT	MDIO Signals to Configure Possible PHYs	I OD CMOS	1.8V Runtime	nc	Not supported on SXAS
S47	GND	Power Ground	PWR GND	—	—	—
S48	I2C_GP_CK	General Purpose I2C Clock Signal	I OD CMOS	1.8V Runtime	PU 2.5K	—
S49	I2C_GP_DAT	General Purpose I2C Data Signal	I OD CMOS	1.8V Runtime	PU 2.5K	—

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S50	HDA_SYNC	High Definition Audio Sample synchronization clock to codec	I/O CMOS	1.8V Runtime	27ohm series	—
	I2S2_LRCK	I2S2 Left & Right Synchronization Clock	I/O CMOS	1.8V Runtime	27ohm series	Module Output if CPU acts in Master Mode Module Input if CPU acts in Slave Mode
	SNDW_CLK1	Clock for Soundwire 1 transactions	O CMOS	1.8V Runtime	—	Soundwire not supported on SXAS
S51	HDA_SDO	High Definition Audio data out to codec	O CMOS	1.8V Runtime	27ohm series	—
	I2S2_SDOUT	I2S2 Digital Audio Output	O CMOS	1.8V Runtime	27ohm series	—
	SNDW_DAT1	Soundwire 1 bi-directional PCM audio data lane	I/O CMOS	1.8V Runtime	—	Soundwire not supported on SXAS
S52	HDA_SDI	High Definition Audio data in from codec	I/O CMOS	1.8V Runtime	—	Series termination off module close to codec suggested.
	I2S2_SDIN	I2S2 Digital Audio Input	I CMOS	1.8V Runtime	—	—
	SNDW_DAT0	Soundwire 0 bi-directional PCM audio data lane	I/O CMOS	1.8V Runtime	—	Soundwire not supported on SXAS
S53	HDA_CK	High Definition Audio clock to codec	O CMOS	1.8V Runtime	27ohm series	—
	I2S2_CK	I2S2 Digital Audio Clock	I/O CMOS	1.8V Runtime	27ohm series	Module Output if CPU acts in Master Mode. Module Input if CPU acts in Slave Mode
	SNDW_CLK0	Clock for Soundwire 0 transactions	O CMOS	1.8V Runtime	—	Soundwire not supported on SXAS
S54	SATA_ACT#	SATA Activity Indicator	O OD CMOS	3.3V Runtime	PU 10K	able to sink 24mA Carrier LED current
S55	USB5_EN_OC#	USB Over-Current Sense for Port 5	I/O OD CMOS	3.3V Standby	PU 10K	Pulled low by Module OD driver to disable USB0 power. Pulled low by Carrier OD driver to indicate over-current situation.
S56	ESPI_IO_2	ESPI Master Data Input / Output	I/O CMOS	1.8V Standby	—	—
	QSPI_IO_2	QSPI Data input / output	I/O CMOS	1.8V Standby	—	QSPI option not supported on SXAS

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S57	ESPI_IO_3	ESPI Master Data Input / Output	I/O CMOS	1.8V Standby	—	—
	QSPI_IO_3	QSPI Data input / output	I/O CMOS	1.8V Standby	—	QSPI option not supported on SXAS
S58	ESPI_RESET#	ESPI Reset	O CMOS	1.8V Standby	PD 75K	Reset the eSPI interface for both master and slaves.
S59	USB5+	USB Differential Data Pairs for Port 5	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
S60	USB5-		I/O USB	USB		—
S61	GND	Power Ground	PWR GND	—	—	—
S62	USB3_SSTX+	Transmit Signal Differential Pairs for SuperSpeed on Port 3	O USB SS	Standby	—	series AC coupled on Module (100nF)
S63	USB3_SSTX-					
S64	GND	Power Ground	PWR GND		—	—
S65	USB3_SSRX+	Receive Signal Differential Pairs for SuperSpeed on Port 3	I USB SS	Standby	—	series AC coupled off Module
S66	USB3_SSRX-					
S67	GND	Power Ground	PWR GND	—	—	—
S68	USB3+	USB Differential Data Pairs for Port 3	I/O USB	USB	PD 14.25K to 24.8K in PCH	—
S69	USB3-		I/O USB	USB		—
S70	GND	Power Ground	PWR GND	—	—	—
S71	USB2_SSTX+	Transmit Signal Differential Pairs for SuperSpeed on Port 2	O USB SS	Standby	—	series AC coupled on Module (100nF)
S72	USB2_SSTX-					
S73	GND	Power Ground	PWR GND	—	—	—
S74	USB2_SSRX+	Receive Signal Differential Pairs for SuperSpeed on Port 3	I USB SS	Standby	—	series AC coupled off Module
S75	USB2_SSRX-					
S76	PCIE_B_RST#	PCIe Port B reset output	O CMOS	3.3V Runtime	PD 10K	Copy of PCH PLTRST#
S77	PCIE_C_RST#	PCIe Port C reset output	O CMOS	3.3V Runtime	PD 10K	Copy of PCH PLTRST#
S78	PCIE_C_RX+ /	Differential PCIe link C receive data pair	I PCIE	Runtime	—	Series AC coupled off Module 75-265nF depending on PCIe generation
	SERDES_1_RX+	Differential SERDES 1 Receive Data Pair	I PCIE	Runtime	—	SERDES option not supported on SXAS

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S79	PCIE_C_RX- /	Differential PCIe link C receive data pair	I PCIE	Runtime	—	Series AC coupled off Module 75-265nF depending on PCIe generation
	SERDES_1_RX-	Differential SERDES 1 Receive Data Pair	I PCIE	Runtime	—	SERDES option not supported on SXAS
S80	GND	Power Ground	PWR GND	—	—	—
S81	PCIE_C_TX+ /	Differential PCIe link C transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
	SERDES_1_TX+	Differential SERDES 1 Transmit Data Pair	O PCIE	Runtime	—	SERDES option not supported on SXAS
S82	PCIE_C_TX- /	Differential PCIe link C transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
	SERDES_1_TX-	Differential SERDES 1 Transmit Data Pair	O PCIE	Runtime	—	SERDES option not supported on SXAS
S83	GND	Power Ground	PWR GND	—	—	—
S84	PCIE_B_REFCK+	Differential PCIe Link B reference clock output	O PCIE	Runtime	—	f = 100MHz
S85	PCIE_B_REFCK-	Differential PCIe Link B reference clock output	O PCIE	Runtime	—	
S86	GND	Power Ground	PWR GND	—	—	—
S87	PCIE_B_RX+	Differential PCIe link B receive data pair	I PCIE	Runtime	—	series AC coupled off Module 75-265nF depending on PCIe generation
S88	PCIE_B_RX-		I PCIE	Runtime	—	
S89	GND	Power Ground	PWR GND	—	—	—
S90	PCIE_B_TX+	Differential PCIe link B transmit data pair	O PCIE	Runtime	—	series AC coupled on Module (220nF)
S91	PCIE_B_TX-		O PCIE	Runtime	—	
S92	GND	Power Ground	PWR GND	—	—	—
S93	DP0_LANE0+	Primary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
S94	DP0_LANE0-		O DP	Runtime	—	
S95	DP0_AUX_SEL	Auxiliary Selection	I CMOS	1.8V Runtime	PD 1M	Pull to GND on Carrier for DP operation Module tolerates high level in stand-by mode
S96	DP0_LANE1+	Primary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
S97	DP0_LANE1-		O DP	Runtime	—	

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S98	DP0_HPD	DP Hot Plug Detect Input	I CMOS	1.8V Runtime	PD 1M	Module tolerates high level in stand-by mode
S99	DP0_LANE2+	Primary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
S100	DP0_LANE2-		O DP	Runtime	—	
S101	GND	Power Ground	PWR GND	—	—	—
S102	DP0_LANE3+	Primary DP Port Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
S103	DP0_LANE3-		O DP	Runtime	—	
S104	USB3_OTG_ID	Input Pin to Announce OTG Device	—	—	nc	Resistor value to ground according to USB specification Insertion on USB 3.2 Port
S105	DP0_AUX+	Primary DP Port Bidirectional Channel used for Link Management and Device Control	I/O DP	3.3V Runtime	PD 100K	If DP1_AUX_SEL=0 (DP mode): AC coupled on module (100nF). If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100K PU. Stronger pull-up is demanded to the Carrier Board.
S106	DP0_AUX-		I/O DP	3.3V Runtime	PU 100K	If DP1_AUX_SEL=0 (DP mode): AC coupled on module (100nF). If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100K PU. Stronger pull-up is demanded to the Carrier Board.
S107	LCD1_BKLT_EN	Secondary Panel Backlight Enable	O CMOS	1.8V Runtime	PD 100K	Only in use when two separate LVDS ports are supported.

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S108	LVDS1_CK+	Secondary LVDS Channel Differential Pair Clock Lines	O LVDS	Runtime	—	—
	eDP1_AUX+	Secondary Bidirectional Channel used for Link Management and Device Control	I/O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_CLK+	Secondary DSI Panel Differential Pair Clock Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S109	LVDS1_CK-	Secondary LVDS Channel Differential Pair Clock Lines	O LVDS	Runtime	—	—
	eDP1_AUX-	Secondary Bidirectional Channel used for Link Management and Device Control	I/O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_CLK-	Secondary DSI Panel Differential Pair Clock Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S110	GND	Power Ground	PWR GND	—	—	—
S111	LVDS1_0+	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX0+	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D0+	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S112	LVDS1_0-	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX0-	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D0-	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S113	eDP1_HPD	Detection of Hot Plug / Unplug of secondary eDP Display and Notification of the Link Layer	I CMOS	1.8V Runtime	nc	Only in use when two separated eDP ports are supported
	DSI1_TE	Secondary DSI Panel Tearing Effect Signal	I CMOS	1.8V Runtime	nc	—
S114	LVDS1_1+	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX1+	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D1+	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S115	LVDS1_1-	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX1-	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D1-	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S116	LCD1_VDD_EN	Secondary Panel Power Enable	O CMOS	1.8V Runtime	PD 100K	Connect to LCD0_VDD_EN on SXAS
S117	LVDS1_2+	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX2+	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D2+	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S118	LVDS1_2-	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX2-	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D2-	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapterfor more details about DSI option
S119	GND	Power Ground	PWR GND	—	—	—
S120	LVDS1_3+	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX3+	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D3+	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S121	LVDS1_3-	Secondary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP1_TX3-	Secondary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	nc	Only in use when two separate eDP ports are supported
	DSI1_D3-	Secondary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S122	LCD1_BKLT_PWM	Secondary Panel Brightness Control	O CMOS	Runtime	—	LCD0_BKLT_PWM
S123	GPIO13	GPIO Pin 13 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
S124	GND	Power Ground	PWR GND	—	—	—
S125	LVDS0_0+	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX0+	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D0+	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S126	LVDS0_0-	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX0-	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D0-	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S127	LCD0_BKLT_EN	Primary Panel Backlight Enable	O CMOS	1.8V Runtime	PD 100K	—
S128	LVDS0_1+	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX1+	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D1+	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S129	LVDS0_1-	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX1-	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D1-	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S130	GND	Power Ground	PWR GND	—	—	—
S131	LVDS0_2+	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX2+	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D2+	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S132	LVDS0_2-	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX2-	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D2-	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S133	LCD0_VDD_EN	Primary Panel Power Enable	O CMOS	1.8V Runtime	PD 100K	—
S134	LVDS0_CK+	Primary LVDS Channel Differential Pair Clock Lines	O LVDS	Runtime	—	—
	eDP0_AUX+	Primary Bidirectional Channel used for Link Management and Device Control	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_CLK+	Primary DSI Panel Differential Pair Clock Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S135	LVDS0_CK+	Primary LVDS Channel Differential Pair Clock Lines	O LVDS	Runtime	—	—
	eDP0_AUX+	Primary Bidirectional Channel used for Link Management and Device Control	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_CLK+	Primary DSI Panel Differential Pair Clock Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S136	GND	Power Ground	PWR GND	—	—	—
S137	LVDS0_3+	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX3+	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D3+	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S138	LVDS0_3-	Primary LVDS Channel Differential Pair Data Lines	O LVDS	Runtime	—	—
	eDP0_TX3-	Primary 4-Lane eDP Differential Pair Data Lines	O DP	Runtime	—	AC coupled off Module (100nF)
	DSI0_D3-	Primary DSI Panel Differential Pair Data Lines	O D-PHY	Runtime	—	See corresponding chapter for more details about DSI option
S139	I2C_LCD_CK	DDC Clock Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V Runtime	PU 2.2K	—
S140	I2C_LCD_DAT	DDC Data Line Used for Flat Panel Detection and Control	I/O OD CMOS	1.8V Runtime	PU 2.2K	—
S141	LCD0_BKLT_PWM	Primary Panel Brightness Control	O CMOS	1.8V Runtime	—	—
S142	GPIO12	GPIO Pin 12 Preferred Input	I/O CMOS	1.8V Runtime	PU 499K	—
S143	GND	Power Ground	PWR GND	—	—	—
S144	eDP0_HPD	Detection of Hot Plug / Unplug of Primary eDP Display and Notification of the Link Layer	I CMOS	1.8V Runtime	PD 1M	Module tolerates high level in stand-by mode
	DSI0_TE	Primary DSI Panel Tearing Effect Signal	I CMOS	1.8V Runtime	PD 1M	See corresponding chapter for more details about DSI option
S145	WDT_TIME_OUT#	Watch-Dog-Timer Output, low active	O CMOS	1.8V Runtime	—	—
S146	PCIE_WAKE#	PCIe wake up interrupt to host	I OD CMOS	3.3V Standby	PU 10K	common to PCIe links A, B, C, D
S147	VDD_RTC	Low current RTC circuit backup power	Analog	2.3V to 3.25V	—	3.0V nominal May be sourced from a Carrier based lithium cell or super cap.
S148	LID#	Lid open/close indication to Module	I OD CMOS	1.8 to 5 V	PU 10K (3.3V)	Driven by OD on Carrier.
S149	SLEEP#	Sleep indicator from Carrier Board	I OD CMOS	1.8 to 5 V	PU 10K (3.3V)	Driven by OD on Carrier.

Pin	Primary (Top) Side	Description	Type	I/O Domain	Module Termination	Comment
S150	VIN_PWR_BAD#	Power bad indication from Carrier Board	I OD CMOS	VDD_IN	PU 10K	Driven by OD on Carrier Module and Carrier power supplies shall not be enabled while this signal is held low by the Carrier.
S151	CHARGING#	Held low by Carrier during battery charging	I OD CMOS	1.8 to 5 V	PU 10K (3.3V)	Driven by OD on Carrier.
S152	CHARGER_PRSNT#	Held low by Carrier if DC input for battery charger is present.	I OD CMOS	1.8 to 5 V	PU 10K (3.3V)	Driven by OD on Carrier.
S153	CARRIER_STBY#	The Module shall drive this signal low when the system is in a standby power state.	O CMOS	1.8V Standby	PD 10K	Copy of PCH SLP_S3# signal
S154	CARRIER_PWR_ON	Carrier Board circuits should not be powered up until the Module asserts the CARRIER_PWR_ON signal.	O CMOS	1.8V Standby	PD 10K	Copy of PCH RSMRST# signal
S155	FORCE_RECOV#	For x86 systems this signal may be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.	I OD CMOS	1.8V Standby	PU 10K	Not supported on SXAS Driven by OD on Carrier
S156	BATLOW#	Battery low indication to Module. Carrier to float the line in inactive state.	I OD CMOS	1.8 to 5V	PU 10K (3.3V)	Driven by OD on Carrier
S157	TEST#	Held Low by Carrier to Invoke Module Vendor Specific Test Functions	I OD CMOS	1.8 to 5V	PU 10K (3.3V)	Carrier Board should leave this pin floating for normal operation.
S158	GND	Power Ground	PWR GND	—	—	—

Table 33: SMARC Connector bottom side

5. UEFI BIOS

5.1 Starting the UEFI BIOS

The SMARC-sXAS uses a JUMPtec-customized, pre-installed and configured version of AMI Aptio® V BIOS based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI.
The UEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the SMARC-sXAS.

This chapter provides an overview of the BIOS and its setup. A more detailed listing and description of all BIOS setup nodes can be found in the BIOS file package available on our Customer Section. Please register there to get access to BIOS downloads and Product Change Notifications.

The UEFI BIOS comes with a Setup program that provides quick and easy access to the individual function settings for control or modification of the default configuration. The Setup program allows access to various menus resp. sub-menus that provide the specific functions.
To start the UEFI BIOS Setup program, follow the steps below:

1. Power on the board
2. Wait until the first characters appear on the screen (POST messages or splash screen)
3. Press the <DEL> key
4. If the UEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password
5. The Setup menu appears

5.2 Navigating the UEFI BIOS

The SMARC-sXAS UEFI BIOS Setup program uses a hot key navigation system with a corresponding legend bar displayed on the setup screens. The following table provides a list of navigation hot keys available in the legend bar.

Hot Key	Description
<F1>	<F1> key invokes the General Help window
< - >	<Minus> key selects the next lower value within a field
<+>	<Plus> key selects the next higher value within a field
<F2>	<F2> key loads previous values
<F3>	<F3> key loads optimized defaults
<F4>	<F4> key Saves and Exits
<←> or <→>	<Left/Right> arrows select major Setup menus on menu bar, for example, Main or Advanced
<↑> or <↓>	<Up/Down> arrows select fields in the current menu, for example, Setup function or sub-screen
<ESC>	<ESC> key exits a major Setup menu and enters the Exit Setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level
<RETURN>	<RETURN> key executes a command or selects a sub-menu

Table 34: Navigation Hot Keys Available in the Legend Bar

5.3 Setup Menus

The Setup utility features a selection bar at the top of the screen that lists the menus

Figure 5: Setup Menu Selection Bar

The Setup menus available for the SMARC-sXAS are:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The currently active menu is highlighted in grey, the currently active UEFI BIOS Setup item in white. Use the left and right arrow keys to select the Setup menu.
Each Setup menu provides two main frames. The left frame displays all available functions and configurable ones are displayed in blue. Functions displayed in grey provide information about the status or the operational configuration.

5.4 Getting Help

The right frame displays a help window. The help window provides an explanation of the respective function.

5.5 UEFI Shell

The JUMPtec UEFI BIOS features a built-in and enhanced version of the UEFI Shell. For a detailed description of the available standard shell scripting, refer to the EFI Shell User Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage: http://sourceforge.net/projects/efi-shell/files/documents/.

JUMPtec UEFI BIOS does not provide all shell commands described in the EFI Shell Command Manual.

5.5.1 Entering the UEFI Shell

To enter the UEFI Shell, follow the steps below:

1. Power on the board
2. Press the <F7> key (instead of <DEL>) to display a choice of boot devices
3. Select 'UEFI: Built-in EFI shell'

```
UEFI Interactive Shell v2.2
EDK II / JUMPtec add-on v0.3
UEFI v2.80 (American Megatrands, 0x0005001A)
map: No mapping found.
```

1. Press the <ESC> key within 5 seconds to skip startup.nsh or any other key to continue
2. The output produced by the device-mapping table can vary depending on the board's configuration
3. If the <ESC> key is pressed before the 5 second timeout elapses, the shell prompt is shown:

```
Shell>
```

5.5.2 Exiting the UEFI Shell

To exit the UEFI Shell, follow one of the steps below:

- Use the **exit** UEFI Shell command to select the boot device, in the Boot menu, that the OS boots from
- Reset the board using the **reset** UEFI Shell command
- Press the reset button of the board or power down/up the board

5.6 UEFI Shell Scripting

5.6.1 Startup Scripting

If the <ESC> key is not pressed and the timeout has run out, then the UEFI Shell automatically tries to execute some startup scripts. The UEFI shell searches for scripts and executes them in the following order:

1. Initially searches for JUMPtec flash-stored startup script
2. If there is no JUMPtec flash-stored startup script present, then the UEFI-specified **startup.nsh** script is used. This script must be located on the root of any of the attached FAT-formatted disk drives
3. If none of the startup scripts are present or the startup script terminates then the default boot order is continued

5.6.2 Create a Startup Script

Startup scripts can be created using the UEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice.

5.6.3 Example of Startup Scripts

Execute Shell Script on other Harddrive

This example (**startup.nsh**) executes the shell script named **bootme.nsh** located in the root of the first detected disk drive (**fs0**).

```
fs0:
bootme.nsh
```

5.7 Firmware Update

Firmware updates are typically delivered as a ZIP archive. Please find the latest available BIOS-ZIP archive on JUMPtec's Customer Section. Further information about the firmware update procedure can be found in the included “flash_instruction.txt”-file.

Register to JUMPtec's Customer Section to get access to BIOS downloads, additional documentation and Product Change Notification service.

6. Technical Support

For technical support contact our Support Department:

E-Mail:	techsupport@jumptec.com

Make sure you have the following information available when contacting us:

- Product ID Number (PN)
- Serial Number (SN)
- Module’s revision
- Operating System and Kernel/Build version
- Software modifications
- Additional connected hardware/full description of hardware set up

The Serial Number can be found on the Type Label, located on the product.

Be ready to explain the nature of your problem to the service technician.

6.1 Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law.

If there is a protection label on your product, then the warranty is lost if the product is opened.

6.2 Returning Defective Material

All equipment returned to JUMPtec must have a Return of Material Authorization (RMA) number assigned exclusively by JUMPtec. JUMPtec cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to JUMPtec’s designated facility. JUMPtec will pay the return freight charges back to the buyer’s location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to JUMPtec:

1. Visit the RMA Information website: RMA Information - JUMPtec
2. Download the RMA Request sheet and fill out the form. Take care to include a short detailed description of the observed problem or failure and to include the product identification information (Name of product, Product Number and Serial Number). If a delivery includes more

than one product, fill out the above information in the RMA Request form for each product.

3. Send the completed RMA-Request form to the fax or email address given at JUMPtec GmbH. JUMPtec GmbH will provide an RMA-Number within one business day.
4. The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to JUMPtec GmbH in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

5. Include the RMA-Number with the shipping paperwork and send the product to the delivery address provided in the RMA form or received from JUMPtec RMA Support.

7. Document Revision

The following table shows the revision of this document.

Revision	Author	Date	Comment
0.1	BaH	2024-04-xx	initial preliminary release
0.2	BaH	2025-01-xx	latest updates
0.3	BaH	2025-02-xx	preliminary release
0.4	BaH	2025-04-22	SPI chapter amended
1.0	BaH	2025-08-20	released

Table 35: Document Revision Table

List of Acronyms

ACPI	Advanced Configuration and Power Interface
COM	Computer-on-Module
CPLD	Complex Programmable Logic Device
ECC	Error Checking and Correction
DDI	Digital Display Interface
DDR4	Double Data Rate Gen 4
DIMM	Dual In-line Memory Module
DP	Display Port
eDP	embedded Display Port
EDID	Extended Display Identification Data
GbE	Gigabit Ethernet
GOIO	General Purpose IO
GPU	Graphics Processing Unit
GSS	Global Sales Support
HD/HDD	Hard Disk /Drive
HDMI	High Definition Multimedia Interface
HSIO	High Speed IO
HWM	Hardware Monitor
I2C	Inter-Integrated Circuit
IOL	IPMI-Over-LAN
IOT	Internet of Things
IPMI	Intelligent Platform Management Interface
LPS	Limited Power Source
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control (Ethernet layer)
MCP	Multi Chip Package
MEI	Management Engine Interface
NA	Not Applicable
PCH	Platform Controller Hub
PCIe	PCI-Express®
PECI	Platform Environment Control Interface
PEG	PCI-Express® Graphics
PHY	Physical Ethernet Layer
PICMG®	PCI Industrial Computer Manufacturers Group
PSE	Programmable Service Engine
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SELV	Safety Extra Low Voltage
SGMII	Serial Gigabit Media Independent Interface
SIO	Super IO
SMBus	System Management Bus
SOC	System on Chip
SOL	Serial Over LAN
SPI	Serial Peripheral Interface

TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface

Table 36: List of Acronyms